




**SPECIFICATION SHEET**

<b>SPECIFICATION SHEET NO.</b>	N0723- 0603N471J101SD
<b>DATE</b>	July 23, 2021
<b>REVISION</b>	A0
<b>DESCRIPTION</b>	Multilayer Ceramic Chip Capacitors 0603 (1608 Metric) Series, L1.60*W0.80*H0.80mm, Dielectric NP0, Capacitance 470pF, Tolerance ±5%, Rated Voltage 100V Operating Temp. Range -55°C ~+125°C Package in Tape/Reel, 4,000pcs/Reel RoHS/RoHS III compliant
<b>CUSTOMER</b>	
<b>CUSTOMER PART NUMBER</b>	
<b>CROSS REF. PART NUMBER</b>	
<b>ORIGINAL PART NUMBER</b>	Aillen 0603N471J101SD
<b>PART CODE</b>	0603N471J101SD

<b>VENDOR APPROVE</b>			
Issued/Checked/Approved			
DATE: July 23 21, 2021			

<b>CUSTOMER APPROVE</b>	
DATE:	

## MULTILAYER CERAMIC CHIP CAPACITORS 0603 SERIES

### MAIN FEATURE

- RoHS III Compliant
- Wide Operating Temperature Range -55~+125°C
- High Capacitance in small size
- Small L1.60\*W0.80\*H0.80mm, 2 Pads

### APPLICATION

- General Digital Circuit
- Power Supply by pass capacitors
- Consumer Electronics
- Telecommunication

**RFQ**  
Request For Quotation

### PART CODE GUIDE

0603	N	471	J	101	S	D
1	2	3	4	5	6	7

- 1) **0603**: Series code for Multilayer Ceramic Chip Capacitors, Dimension L1.60\*W0.80\*H0.80mm, 0603 (1608 Metric) Series
- 2) **N**: Dielectric code NPO
- 3) **471**: Capacitance Code, Two significant digits followed by number of Zero, The 3rd digit signifies the multiplying factor, and letter R is decimal point, Example: 471 = 470pF
- 4) **J**: Capacitance Tolerance code, K: +/-10%; J: +/-5%
- 5) **101**: Rated Voltage Code: Two significant digits followed by number of Zero and letter R is decimal point, 101= 100 VDC
- 6) **S**: Thickness code, 0.80+/-0.10mm
- 7) **D**: Tape/Reel code, Packed in Tape/Reel. 4,000pcs/Reel

**MULTILAYER CERAMIC CHIP CAPACITORS 0603 SERIES**

**DIMENSION (Unit: mm)**

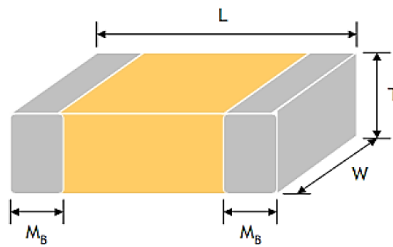


Image for reference



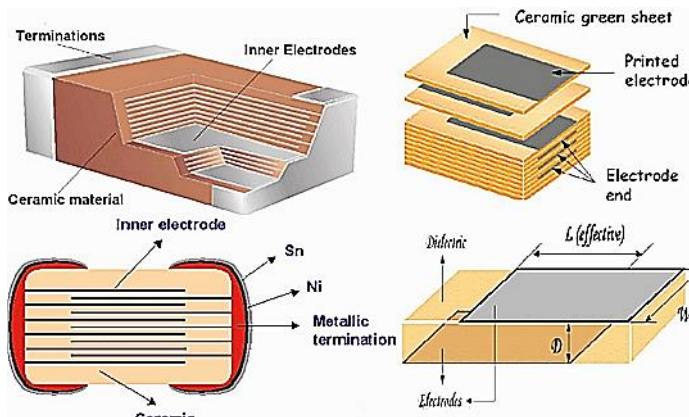
Marking: Blank

0603



Item	Dimension
L	1.60±0.20
W	0.80±0.20
T	0.80±0.10
M B	0.40±0.15

**MLCC construction for Reference**



**MULTILAYER CERAMIC CHIP CAPACITORS 0603 SERIES**

**GENERAL ELECTRONICAL CHARACTERISTICS**

Item	Unit	Symbol	Characteristic	Condition
Size		0603	Dimension L1.60*W0.80*H0.80mm, 0603 (1608 Metric) Series	
Dielectric		N	NPO	
Capacitance Range	pF	471	470	
Capacitance Tolerance	%	J	±5	
Rated Voltage	VDC	101	100	
Operating Temperature	°C		-55 ~+125	
Capacitance Characteristic	ppm		±30	
Termination			Ni/Sn (Lead- Free)	

**MULTILAYER CERAMIC CHIP CAPACITORS 0603 SERIES**

**RELIABILITY TEST CONDITIONS AND REQUIREMENTS**

Item	Test Condition	Requirements
<b>Visual and Mechanical</b>	-	No remarkable defect. Dimensions to conform to individual specification sheet.
<b>Capacitance</b>	Class I: (NPO) $C \leq 1000\text{pF}$ , $1.0 \pm 0.2V_{rms}$ , $1\text{MHz} \pm 10\%$ ** Test condition:	* Shall not exceed the limits given in the detailed spec.
<b>Q/D.F. (Dissipation Factor)</b>	$0.5 \pm 0.2V_{rms}$ , $1\text{KHz} \pm 10\%$	NPO: Capacitance $\geq 30\text{pF}$ , $Q \geq 1000$ ;
<b>Dielectric Strength</b>	* To apply voltage ( $\leq 100\text{V}$ ) 250%. * Duration: 1 to 5 sec. * Charge and discharge current less than 50mA.	No evidence of damage or flash over during test.
<b>Insulation Resistance</b>	* Preconditioning for Class II MLCC: Perform a heat treatment at $150 \pm 10^\circ\text{C}$ for 1 hour, then leave in ambient condition for $24 \pm 2$ hours before measurement. To apply rated voltage for max. 120 sec.	Class I (NPO) $10G\Omega$ or $RxC \geq 500\Omega\text{-F}$ whichever is smaller.
<b>Temperature Coefficient</b>	With no electrical load, Operating Temp. $-55 \sim 125^\circ\text{C}$ at $25^\circ\text{C}$	Operating Temperature tolerance: $\pm 30\text{ppm}/^\circ\text{C}$

**MULTILAYER CERAMIC CHIP CAPACITORS 0603 SERIES**
**RELIABILITY TEST CONDITIONS AND REQUIREMENTS**

Item	Test Condition	Requirements
<b>Adhesive Strength of Termination</b>	* Pressurizing force: 5N ( $\leq 0603$ ) * Test time: $10 \pm 1$ sec.	No remarkable damage or removal of the terminations.
<b>Vibration Resistance</b>	* Vibration frequency: 10~55 Hz/min. * Total amplitude: 1.5mm * Test time: 6 hrs. (Two hrs each in three mutually perpendicular directions.)  *Cap./DF(Q) Measurement to be made after de-aging a 150° C for 1hr then set for $24 \pm 2$ hrs at room temp.	* No remarkable damage or removal of the terminations. * No remarkable damage. * Cap change and Q/D.F.: To meet initial spec.
<b>Solder ability</b>	* Solder temperature: $235 \pm 5^{\circ}\text{C}$ * Dipping time: $2 \pm 0.5$ sec.	95% min. coverage of all metalized area.
<b>Bending Test</b>	* The middle part of substrate shall be pressurized by means of the pressurizing rod at a rate of about 1 mm per second until the deflection becomes 1 mm and then the pressure shall be maintained for $5 \pm 1$ sec.  * Measurement to be made after keeping at room temp. for $24 \pm 2$ hrs.	* No remarkable damage. • Cap change: • NPO: within $\pm 5\%$ or 0.5pF whichever is larger  (This capacitance change means the change of capacitance under specified flexure of substrate from the capacitance measured before the test.)
<b>Resistance to Soldering Heat</b>	* Solder temperature: $260 \pm 5^{\circ}\text{C}$ * Dipping time: $10 \pm 1$ sec  * Preheating: 120 to 150° C for 1 minute before immerse the capacitor in a eutectic solder.  *Cap. / DF(Q) / I.R. Measurement to be made after de-aging at 150°C for 1hr then set for $24 \pm 2$ hrs at room	* No remarkable damage. * Cap change: NPO: within $\pm 2.5\%$ or 0.25pF whichever is larger  * Q/D.F., I.R. and dielectric strength: To meet initial requirements.  * 25% max. leaching on each edge.

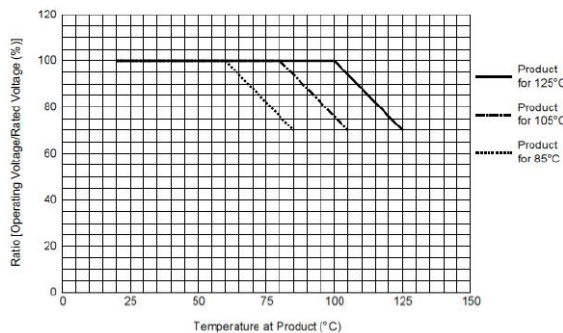
**MULTILAYER CERAMIC CHIP CAPACITORS 0603 SERIES**

**RELIABILITY TEST CONDITIONS AND REQUIREMENTS**

Item	Test Condition	Requirements
<b>Temperature Cycle</b>	<p>* Conduct the five cycles according to the temperatures and time.</p> <p>Step 1: Time: 30+/-3 Minutes@+0/-3 °C Min.            Step 2: Time: 2~3 Minutes@+25 °C            Step 3: Time: 30+/-3 Minutes@+3/-0 °C Max.            Step 4: Time: 2~3 Minutes@+25 °C</p> <p>* Cap. / DF(Q) / I.R. Measurement to be made after de-aging at 150°C for 1hr then set for 24 ± 2 hrs at room.</p>	<p>* No remarkable damage.            * Cap change: NP0: within ± 2.5% or 0.25pF whichever is larger</p> <p>* Q/D.F., I.R. and dielectric strength: To meet initial requirements.</p>
<b>Humidity (Damp Heat) Steady State</b>	<p>* Test temp.: 40 ± 2 ° C            * Humidity: 90~95% RH            * Test time: 500+24/-0hrs.</p> <p>* Cap. / DF(Q) / I.R. Measurement to be made after de-aging at 150 ° C for 1hr then set for 24 ± 2 hrs at room temp.</p>	<p>* No remarkable damage.            * Cap change: NP0: within ± 2.5% or 0.25pF whichever is larger</p> <p>* Q/D.F. value: NP0: More than 30pF,Q ≥350</p>
<b>Humidity (Damp Heat) Load</b>	<p>* Test temp.: 40±2°C            * Humidity: 90~95%RH            * Test time: 500+24/-0 hrs.            * To apply voltage: rated voltage.</p> <p>* Cap. / DF(Q) / I.R. Measurement to be made after de-aging at 150°C for 1hr.then set for 24±2 hrs at room temp</p>	<p>* No remarkable damage.            * Cap change: NP0: ±7.5% or 0.75pF whichever is larger</p> <p>* Q/D.F. value: NP0: More than 30pF,Q ≥200,</p>

**MULTILAYER CERAMIC CHIP CAPACITORS 0603 SERIES**

**RELIABILITY TEST CONDITIONS AND REQUIREMENTS**

Item	Test Condition	Requirements
<p><b>High Temperature Load (Endurance)</b></p>	<p>*Test temp.: NPO: <math>125 \pm 3^\circ\text{C}</math></p> <p>*Test time: 1000+24/-0 hrs.</p> <p>*To apply voltage: <math>10\text{V} \leq U_r &lt; 500\text{V}</math>: 200% of rated voltage.</p> <p>* Cap. / DF(Q) / I.R. Measurement to be made after de-aging at <math>150^\circ\text{C}</math> for 1hr then set for <math>24 \pm 2</math> hrs at room temp.</p> <p>** De-rating conditions</p>  <p>The graph shows the de-rating curve for the capacitors. The y-axis is 'Ratio (Operating Voltage/Rated Voltage [%])' ranging from 0 to 120. The x-axis is 'Temperature at Product (°C)' ranging from 0 to 150. Three curves are shown: a solid line for 125°C, a dashed line for 105°C, and a dotted line for 85°C. All curves start at 100% at 25°C. The 125°C curve remains at 100% until 100°C, then drops to ~70% at 125°C. The 105°C curve remains at 100% until 75°C, then drops to ~70% at 100°C. The 85°C curve remains at 100% until 50°C, then drops to ~70% at 75°C.</p>	<p>* No remarkable damage.</p> <p>* Cap change: NPO: <math>\pm 3.0\%</math> or <math>0.30\text{pF}</math> whichever is larger</p> <p>* Q/D.F. value: NPO: More than <math>30\text{pF}, Q \geq 350</math>,</p>



## MULTILAYER CERAMIC CHIP CAPACITORS 0603 SERIES

### STORAGE AND HANDLING CONDITIONS

- (1) To store products at 5 to 40°C ambient temperature and 20 to 70% related humidity conditions.
- (2) The product is recommended to be used within one year after shipment. Check solder ability in case of shelf life extension is needed.
- (3) Don't open the tape until the parts are to be used, use the chips within 3 months after the tape is opened.
- (4) For product of high dielectric constant (Class2&3, characteristics B/W & Y), the Electro static capacity changes with the passage of time due to the inherent characteristics of ceramic dielectric materials. The changed capacity reverts to nominal at the temperature it reaches during the soldering process.

### CAUTIONS

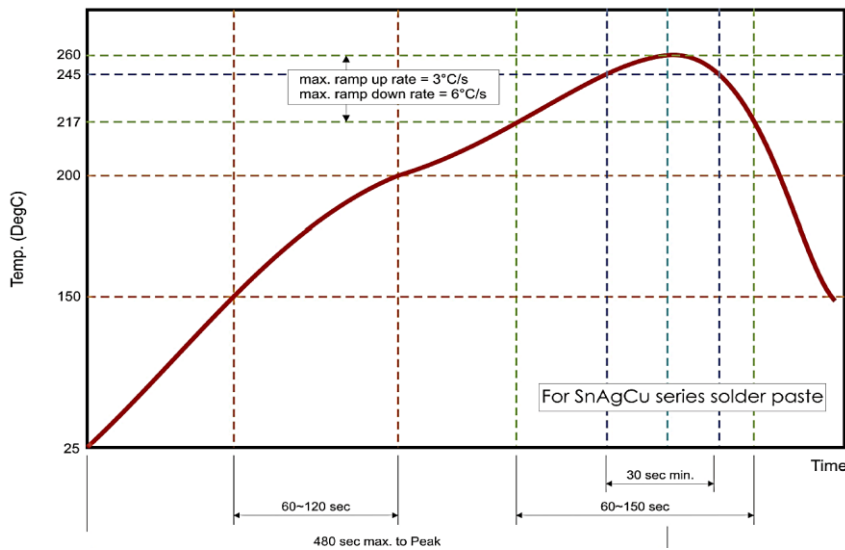
- (1) The corrosive gas reacts on the terminal electrodes of capacitors, and results in the poor solder ability. Do not store the capacitors in the ambience of corrosive gas (e.g., hydrogen sulfide, sulfur dioxide, chlorine, ammonia gas etc.)
- (2) In corrosive atmosphere, solder ability might be degraded, and silver migration might occur to cause low reliability.
- (3) Due to the dewing by rapid humidity change, or the photochemical change of the terminal electrode by direct sun light, the solder ability and electrical performance may deteriorate. Do not store capacitors under direct sunlight or dewing condition. To store products on the shelf and avoid exposure to moisture.

## MULTILAYER CERAMIC CHIP CAPACITORS 0603 SERIES

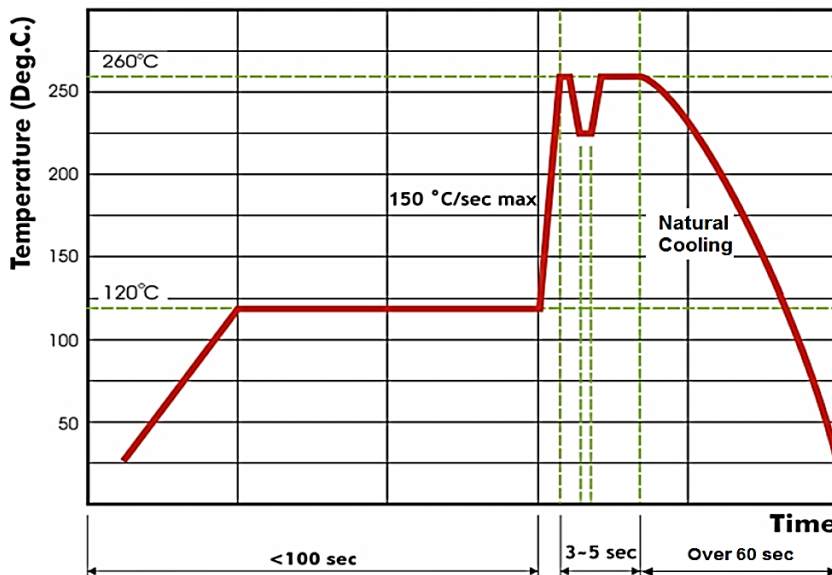
### RECOMMENDED PROFILE CONDITIONS

The lead-free termination MLCCs are not only to be used on SMT against lead-free solder paste, but also suitable against lead-containing solder paste.

If the optimized solder joint is requested, increasing soldering time, temperature and concentration of N2 within oven are recommended.



Reflow Soldering Profile For SMT Process with SnAgCu series Solder Paste

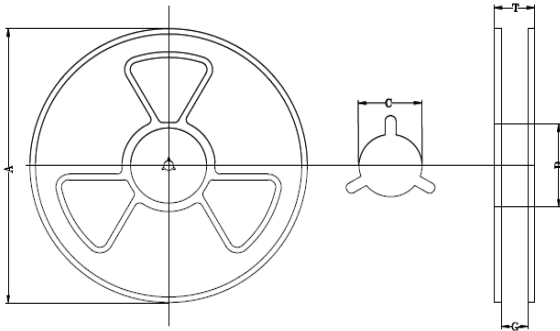


Wave Soldering Profile For SMT Process with SnAgCu series Solder Paste

**MULTILAYER CERAMIC CHIP CAPACITORS 0603 SERIES**

**REEL DIMENSION (Unit: mm)**

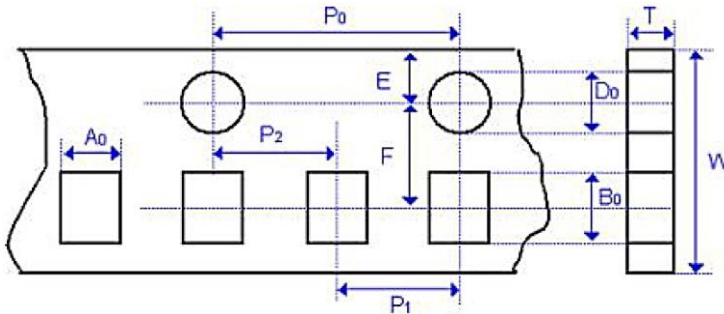
7": 4,000Ppcs/Reel



Code	Dimension 7"	Dimension 10"	Dimension 13"
A	<b>178.0+/-0.1</b>	250.0+/-1.0	330.0+/-1.0
B	<b>60.0 Min.</b>	100.0 Min.	100.0 Min.
C	<b>13.0+/-0.50</b>	13.0+/-0.50	13.0+/-0.50
G	<b>8.4+/-1.0</b>	8.4+/-1.0	8.4+/-1.0

**TAPE DIMENSION (Unit: mm)**

Paper Tape



Code	Dimension
A 0	1.05+/-0.30
B 0	1.80+/-0.30
T	1.20 Max.
K 0	-
W	8.00+/-0.30
P 0	4.00+/-0.10
10xP 0	40.0+/-0.20
P 1	4.00+/-0.10
P 2	2.00+/-0.05
D 0	1.50+/-0.10
D 1	-
E	1.75+/-0.10
F	3.50+/-0.05

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